the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

C1 end

at least one state machine for controlling the at least one interface unit.

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3 ~~23~~. (Twice Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

C2

an address generator in communication with the processing unit, the address generator generating an address for selecting a unit coupled to the bus system.

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4 ~~24~~. (Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

C3

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

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a second plurality of lines coupled to the at least one interface unit, the second plurality of lines for at least one of reading data and writing data.

5
~~25~~. (Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

at least one internal bus system coupled to the at least one interface unit, the at least one internal bus system including a plurality of individual lines, the at least one internal bus system for at least one of reading data and writing data.

C3

6
~~26~~. (Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

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at least one register coupled to the plurality of lines for managing and controlling the bus system.

7
~~27.~~ (Amended) [The]A bus system [of claim 20], [the bus system further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; ~~and~~

C3 end

a bus master unit coupled to the plurality of lines for controlling the bus system; and

a plurality of slave units in communication with the bus master unit.

10
~~30~~. (Twice Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

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a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

a register in communication with the at least one interface unit, the register indicating whether data is stored

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C4 end in the at least one interface unit.

14 ~~34~~. (Twice Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

C5 at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

at least one connection to at least one of a data flow processor (DFP), a field programmable gate array (FPGA), and a dynamically programmable gate array (DPGA).

16 ~~35~~. (Amended) The bus system according to claim [19] 15 ~~37~~, wherein the memory device is external to the processing unit.

18 ~~36~~. (Amended) The bus system according to claim [20] 17 ~~38~~, wherein the memory device is external to the processing unit.

C6 15 ~~37~~. (Amended) [The] A bus system [according to claim 19], [wherein] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture, the processing unit [includes] including a plurality of re-programmable, dynamically reconfigurable cells; and

a plurality of individual lines positioned within the processing unit, the plurality of individual lines being bundled;

wherein the plurality of individual lines provide communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and

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iii) a peripheral device.

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~~38~~. (Amended) [The] A bus system [according to claim 20], [wherein] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture, the processing unit [includes] including a plurality of re-programmable, dynamically reconfigurable cells;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled; and

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

C6 end

Please add the following new claims:

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~~39~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a bus positioned within the processing unit;

at least one interface unit coupled to the bus, the bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

C7

at least one state machine for controlling the at least one interface unit.

20
~~40~~. (New) The bus system of claim 19 ~~39~~, wherein the at least one state machine controls an external bus.

21
~~41~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

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a bus positioned within the processing unit;

at least one interface unit coupled to the bus, the bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

an address generator in communication with the processing unit, the address generator generating an address for selecting a unit coupled to the bus.

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~~42~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit;

at least one interface unit coupled to the first bus, the first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

C7

a second bus coupled to the at least one interface unit, the second bus for at least one of reading data and writing data.

23
~~43~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit;

at least one interface unit coupled to the first bus, the first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

at least one internal bus system coupled to the at least one interface unit, the at least one internal bus system for at least one of reading data and writing data.

24
~~44~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit;

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at least one interface unit coupled to the bus, the first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

at least one register coupled to the first bus for managing and controlling the bus system.

25
~~45~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit;

at least one interface unit coupled to the first bus, the first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

a bus master unit coupled to the first bus for controlling the bus system; and

a plurality of slave units in communication with the bus master unit.

C7

26
~~46~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit, the first bus providing communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a peripheral device;

at least one interface unit coupled to the first bus;

a bus master unit coupled to the first bus and controlling the bus system; and

a plurality of slave units in communication with the bus master unit;

wherein control of the bus system is transferred dynamically from the bus master unit to another unit coupled to the bus system.

40

27 ~~47~~. (New) The bus system of claim 26 ~~46~~, wherein at least one of the plurality of slave units request control of the bus system.

28 ~~48~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the first bus, first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

a register in communication with the at least one interface unit, the register indicating whether data is stored in the at least one interface unit.

29 ~~49~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit, the first bus providing communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a peripheral device; and

at least one interface unit coupled to the first bus, the at least one interface unit being at least one of integral with the processing unit and formed by a configuration of a plurality of logic cells, each of the plurality of logic cells implementing simple logical functions according to a logic cell configuration.

30 ~~50~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit, the first bus providing communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a

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peripheral device; and

at least one interface unit coupled to the first bus, the at least one interface unit being configured by at least one of a primary logic unit and the processing unit.

31 ~~51~~. (New) The bus system of claim 30 ~~50~~, wherein the primary logic unit is at least partially integrated with the processing unit.

32 ~~52~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first bus positioned within the processing unit;

at least one interface unit coupled to the first bus, the first bus providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and

at least one connection to at least one of a data flow processor (DFP), a field programmable gate array (FPGA), and a dynamically programmable gate array (DPGA).

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33 ~~53~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture, the processing unit including a plurality of re-programmable, dynamically reconfigurable cells; and

a bus positioned within the processing unit;

wherein the bus provides communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

34 ~~54~~. (New) The bus system according to claim 33 ~~53~~, wherein the memory device is external to the processing unit.

35 ~~55~~. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-

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